REMARKS

To date, the Examiner has not indicated that all of the subject matter of the information disclosure statement (IDS) filed October 13, 2005 has been properly considered. A copy of such IDS is submitted herewith. If the Examiner requires additional copies of any reference(s), applicant invites the Examiner to contact the undersigned. Documentation in the file wrapper of the instant application confirming the Examiner's consideration of the reference(s) is respectfully requested.

Applicant conducted a telephonic interview with the Examiner on the above matter, as well as related matters, on December 27, 2005. This response is a follow up to such interview.

During the interview, applicant argued that neither Tanaka (US Patent Number: 6,100,589) nor Suzuki et al. (US Patent Number: 6,707,156) even suggested applicant's claimed "meshed ... metal layer ... disposed, at least partially, directly above the active circuit." In response, the Examiner made reference to Figure 11 from Tanaka below.

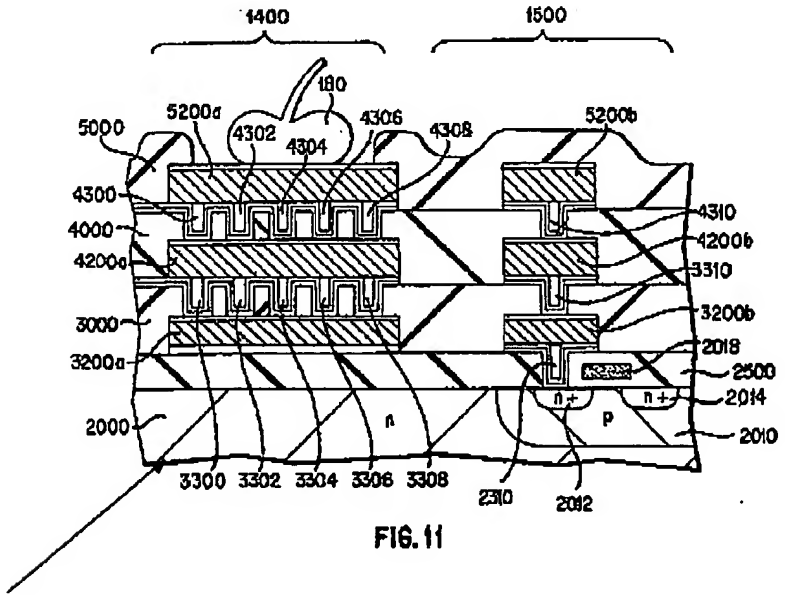

FIG. 11

Specifically, the Examiner argued that the n-type substrate (annotated above) met applicant's claimed "active circuit," since it constituted at least a part of the MOS transistor shown in Fig. 11.

In response to such argument, applicant disagreed, but also suggested amending the claims to define applicant's "active circuit" to include one or more transistors. To this suggestion, the Examiner remained optimistic pending another search. It was thus deemed appropriate for applicant to submit such amendment.

Accordingly, applicant has entered amendments above reflecting the consensus reached during the December 27, 2005 interview. Specifically, now claimed, in each of the independent claims is the following or similar language:

> "wherein the active circuit includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad, and the mesh ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process."

Applicant again emphasizes that simply none of the references relied upon by the Examiner even suggests an entirety of at least one of the transistors being disposed directly below the bond pad, and a mesh that ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process. Again, only applicant teaches and claims a mesh for protecting at least one transistor of an active circuit from damage during a bonding process.

Thus, the Examiner has rejected Claims 1, 3-18, 20, 27, 29, and 30 under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Suzuki et al. This rejection is deemed overcome in view of the amendments made hereinabove.

Specifically, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to

combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

Applicant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to teach or suggest all of the claim limitations, as noted above.

Thus, all of the independent claims are deemed allowable. Moreover, the remaining dependent claims are further deemed allowable, in view of their dependence on such independent claims.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 971-2573. For payment of any additional fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP234/P000825).

Respectfully submitted,

By: _____ Date: 1/05/06

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COPY

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Singh et al.	Group Art Unit: 2811
Application No.: 10/633,004	Examiner: Vu, Hung K.
Filed: 07/31/2003	Atty. Docket No.: NVIDP234/ P000825
For: PAD OVER ACTIVE CIRCUIT SYSTEM AND METHOD WITH MESHED SUPPORT STRUCTURE	Date: October 13, 2005

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents, Alexandria, VA 22313-1450 on the date noted above.

Signed: Erica L. Farlow

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §§ 1.56 AND 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The reference(s) listed in the attached PTO Form 1449, cop(ies) of which is attached (when necessary), may be material to examination of the above-identified patent application. Applicants submit the reference(s) in compliance with their duty of disclosure pursuant to 37 CFR §§ 1.56 and 1.97. The Examiner is requested to make the reference(s) of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that the reference(s) indeed constitutes prior art.

This Information Disclosure Statement is believed to be filed within three months of the filing date of a national application other than a continued prosecution application, within three months of the date of entry of the national stage in an international application, before the mailing of a first Office action on the merits, or before the mailing of a first Office action after the filing of a request for continued examination. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 50-1351 (Order No. NVIDP234).

Respectfully submitted,
Zilka-Kotab, PC

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Form 1449 (Modified) **Information Disclosure Statement By Applicant** (Use Several Sheets if Necessary)	Atty. Docket No. NVIDP234/P000825 Applicant: Singh et al. Filing Date: 07/31/2003	Application No.: 10/633,004 Group Art Unit: 2811

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	L							
	M							
	N							
	O							
	P							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	R	Copy of the Translation of The Antecedent Notification Of Rejection Reasons From Taiwanese Application no. 93114432
	S	
	T	

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.